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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,605	11/13/2001	Chao-Kun Hu	YOR919990336US2	8304

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EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,605	HU ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-10,18-22,24-27 and 35-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-10,18-22,24-27 and 35-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *22 January 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on January 22, 2003 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 37 and 38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. It is not clear in claims 37 and 38 if the metal phosphide-conductive film is the same as the conductive film in claims 1, 2, 18 and 19 respectively. Are there two different conductive films?

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 3, 4, 18, 19, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubin et al. (USPAT 5695810, Dubin) in view of Hong et al. (USPAT 6077774, Hong).

With regard to claims 1 and 3, Dubin discloses in figures 1 – 4 a method for forming conductors with high electromigration resistance. Dubin discloses in figures 1 – 4 forming a layer of dielectric (11) on a substrate. Dubin discloses in figures 1 – 4 forming at least one trench (8) in said layer of dielectric. Dubin discloses in figures 1 – 4 forming a metal liner (15) in said trench. Dubin discloses in figures 1 – 4 forming a conductor (16) on said metal liner filling said trench. Dubin discloses in figures 1 – 4 forming a planarized upper surface of said conductor planar with the upper surface of said layer of dielectric. Dubin discloses in figures 1 – 4 forming a conductive film (17) over said upper surface of said conductor, said conductive film forming a metal to metal metallurgical bond. Dubin does not disclose a thickness for the conductive film. Hong teaches in figure 1f, column 1, lines 32 – 36 and column 5, lines 19 – 23 wherein a conductive film (34) has a thickness of 9 nanometers. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of Hong for the conductive film of Dubin in order to form a diffusion barrier with sufficiently low resistance for

deep submicron copper interconnects as stated by Hong in column 1, lines 32 – 36. Deep submicron copper interconnects are desirable in order increase the speed of the chip.

With regard to claims 2 and 4, Dubin discloses in figures 1 – 4 and column 7, lines 42 – 44 wherein said step of forming a conductive film includes the step of forming said conductive film by electroless deposition whereby said upper surface of said conductor is protected from oxidation and corrosion and provides high electromigration resistance and high resistance to thermal stress voiding.

With regard to claims 18 and 20, Dubin discloses in figures 1 – 4 and column 7, lines 42 – 44 a method for forming conductors with high electromigration resistance. Dubin discloses in figures 1 – 4 and column 7, lines 42 – 44 forming a patterned conductor on a substrate. Dubin discloses in figures 1 – 4 and column 7, lines 42 – 44 forming a conductive film over said surface of said conductor, said conductive film forming a metal to metal metallurgical bond. Dubin does not disclose a thickness for the conductive film. Hong teaches in figure 1f, column 1, lines 32 – 36 and column 5, lines 19 – 23 forming a conductive film (34) over a surface of a conductor (30), the conductive film forming a metal to metal metallurgical bond and has a thickness of 9 nanometers. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of Hong for the conductive film of Dubin in order to form a diffusion barrier with sufficiently low resistance for deep submicron copper interconnects as stated by Hong in column 1, lines 32 – 36. Deep submicron copper interconnects are desirable in order increase the speed of the chip.

With regard to claims 19 and 21, Dubin discloses in figures 1 – 4 and column 7, lines 42 – 44 wherein said step of forming a conductive film includes the step of forming said conductive

film by electroless deposition whereby said surface of said conductor is protected from oxidation and corrosion and provides high electromigration resistance and high resistance to thermal stress voiding.

7. Claims 1, 9, 10, 18, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maydan et al. (USPAT 6372633, Maydan) in view of Hong.

With regard to claim 1, Maydan discloses in figures 2, 3 and 6 – 7 a method for forming conductors with high electromigration resistance. Maydan discloses in figures 2, 3 and 6 – 7 forming a layer of dielectric (22) on a substrate. Maydan discloses in figures 2, 3 and 6 – 7 forming at least one trench (26) in said layer of dielectric. Maydan discloses in figures 2, 3 and 6 – 7 forming a metal liner (28) in said trench. Maydan discloses in figures 2, 3 and 6 – 7 forming a conductor (33) on said metal liner filling said trench. Maydan discloses in figures 2, 3 and 6 – 7 forming a planarized upper surface of said conductor planar with the upper surface of said layer of dielectric. Maydan discloses in figures 2, 3 and 6 – 7 forming a conductive film (34) over said upper surface of said conductor, said conductive film forming a metal to metal metallurgical bond. Maydan does not disclose a thickness for the conductive film. Hong teaches in figure 1f, column 1, lines 32 – 36 and column 5, lines 19 – 23 wherein a conductive film (34) has a thickness of 9 nanometers. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of Hong for the conductive film of Maydan in order to form a diffusion barrier with sufficiently low resistance for deep submicron copper interconnects as stated by Hong in column 1, lines 32 – 36. Deep submicron copper interconnects are desirable in order increase the speed of the chip.

With regard to claim 9, Maydan discloses in figures 2, 3 and 6 – 7, column 4, lines 62 – 67 and column 7, lines 9 – 12 wherein said conductive film is applied on the surface of said conductor by Chemical Vapor Deposition (CVD).

With regard to claim 10, Maydan discloses in figures 2, 3 and 6 – 7, column 4, lines 62 – 67 and column 7, lines 9 – 12 wherein said conductive film is W.

With regard to claim 18, Maydan discloses in figures 2, 3 and 6 – 7 a method for forming conductors with high electromigration resistance. Maydan discloses in figures 2, 3 and 6 – 7 forming a patterned conductor on a substrate. Maydan discloses in figures 2, 3 and 6 – 7 forming a conductive film over said surface of said conductor, said conductive film forming a metal to metal metallurgical bond. Maydan does not disclose a thickness for the conductive film. Hong teaches in figure 1f, column 1, lines 32 – 36 and column 5, lines 19 – 23 forming a conductive film (34) over a surface of a conductor (30), the conductive film forming a metal to metal metallurgical bond and has a thickness of 9 nanometers. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of Hong for the conductive film of Maydan in order to form a diffusion barrier with sufficiently low resistance for deep submicron copper interconnects as stated by Hong in column 1, lines 32 – 36. Deep submicron copper interconnects are desirable in order increase the speed of the chip.

With regard to claim 26, Maydan discloses in figures 2, 3 and 6 – 7 wherein said conductive film is applied on the surface of said conductor by Chemical Vapor Deposition (CVD).

With regard 27, Maydan discloses in figures 2, 3 and 6 – 7 wherein said conductive film is W.

8. Claims 1, 2, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (USPAT 6180523, Lee) in view of Hong.

With regard to claim 1, Lee discloses in figures 1 – 8 a method for forming conductors with high electromigration resistance. Lee discloses in figures 1 – 8 forming a layer of dielectric (20) on a substrate. Lee discloses in figures 1 – 8 forming at least one trench (24) in said layer of dielectric. Lee discloses in figures 1 – 8 forming a metal liner (28) in said trench. Lee discloses in figures 1 – 8 forming a conductor (38) on said metal liner filling said trench. Lee discloses in figures 1 – 8 forming a planarized upper surface of said conductor planar with the upper surface of said layer of dielectric. Lee discloses in figures 1 – 8 forming a conductive film (46) over said upper surface of said conductor, said conductive film forming a metal to metal metallurgical bond. Lee does not disclose a thickness for the conductive film. Hong teaches in figure 1f, column 1, lines 32 – 36 and column 5, lines 19 – 23 wherein a conductive film (34) has a thickness of 9 nanometers. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of Hong for the conductive film of Lee in order to form a diffusion barrier with sufficiently low resistance for deep submicron copper interconnects as stated by Hong in column 1, lines 32 – 36. Deep submicron copper interconnects are desirable in order increase the speed of the chip.

With regard to claim 2, Lee discloses in figures 1 – 8 wherein said step of forming a conductive film includes the step of forming said conductive film by electroless deposition whereby said upper surface of said conductor is protected from oxidation and corrosion and provides high electromigration resistance and high resistance to thermal stress voiding.

With regard to claim 18, Lee discloses in figures 1 – 8 a method for forming conductors with high electromigration resistance. Lee discloses in figures 1 – 8 forming a patterned conductor on a substrate. Lee discloses in figures 1 – 8 forming a conductive film over said surface of said conductor, said conductive film forming a metal to metal metallurgical bond. Lee does not disclose a thickness for the conductive film. Hong teaches in figure 1f, column 1, lines 32 – 36 and column 5, lines 19 – 23 forming a conductive film (34) over a surface of a conductor (30), the conductive film forming a metal to metal metallurgical bond and has a thickness of 9 nanometers. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of Hong for the conductive film of Lee in order to form a diffusion barrier with sufficiently low resistance for deep submicron copper interconnects as stated by Hong in column 1, lines 32 – 36. Deep submicron copper interconnects are desirable in order increase the speed of the chip.

With regard to claim 19, Lee discloses in figures 1 – 8 wherein said step of forming a conductive film includes the step of forming said conductive film by electroless deposition whereby said surface of said conductor is protected from oxidation and corrosion and provides high electromigration resistance and high resistance to thermal stress voiding.

9. Claims 5, 7, 22, 24, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubin and Hong as applied to claims 1, 2, 18 and 19 above, and further in view of Zhao et al (USPAT 5674787, Zhao).

With regard to claims 5 and 22, Dubin discloses in figures 1 – 4 and column 6, lines 36 – 55 wherein said step of electroless deposition includes the steps of first immersing said substrate

in a solution of metal ions whereby a layer of nanoparticles of metal are formed on said upper surface of said conductor. Dubin discloses in figures 1 – 4, column 6, lines 6 – 23 and column 7, lines 42 – 49 second immersing said substrate in an electroless complexed solution of metal ions and hypophosphite ions whereby the conductive film formed comprises a metal-phosphide conductive film on said upper surface of said conductor. Dubin teaches that the metal-phosphide conductive film is a barrier layer. It is not clear if Dubin and Hong teach annealing the metal-phosphide conductive film. Zhao teaches in figure 13; and column 8, lines 63 – 65 annealing a substrate in an inert atmosphere at a temperature of 200° C for 1 hour whereby excellent adhesion is obtained between a conductor (23) and a metal conductive film (24). It would have been obvious to one of ordinary skill in the art at the time of the present invention to anneal the metal-phosphide conductive layer of Dubin and Hong in order to improve the electrical properties of the plugs as stated by Zhao in column 3, lines 30 – 35. Dubin, Hong, and Zhao disclose the claimed invention except for the anneal at a temperature of at least 300° C and a time of at least 2 hours. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the anneal at a temperature of at least 300° C and a time of at least 2 hours, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. It is further obvious in the method of Dubin, Hong, and Zhao that excellent adhesion is obtained between the conductor and the metal-phosphide conductive film during the anneal.

With regard to claims 7 and 24, Dubin teaches in column 7, lines 42 – 45 the conductive film is CoWP.

With regard to claims 37 and 38, Dubin discloses in figures 1 – 4, column 6, lines 6 – 23 and column 7, lines 42 – 49 wherein said electroless deposition comprises immersing said substrate in an electroless complexed solution of metal ions and hypophosphite ions whereby a metal-phosphide conductive film is formed on said upper surface of said conductor. It is not clear if Dubin and Hong teach annealing the metal-phosphide conductive film. Zhao teaches in figure 13; and column 8, lines 63 – 65 annealing a substrate in an inert atmosphere at a temperature of 200° C for 1 hour whereby excellent adhesion is obtained between a conductor (23) and a metal conductive film (24). It would have been obvious to one of ordinary skill in the art at the time of the present invention to anneal the metal-phosphide conductive layer of Dubin and Hong in order to improve the electrical properties of the plugs as stated by Zhao in column 3, lines 30 – 35. Dubin, Hong, and Zhao disclose the claimed invention except for the anneal at a temperature of at least 300° C and a time of at least 2 hours. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the anneal at a temperature of at least 300° C and a time of at least 2 hours, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. It is further obvious in the method of Dubin, Hong, and Zhao that excellent adhesion is obtained between the conductor and the metal-phosphide conductive film during the anneal.

10. Claims 8, 25, 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee and Hong as applied to claims 1, 2, 18 and 19 above, and further in view of Zhao.

With regard to claims 8 and 25, Lee discloses in figures 1 – 8 wherein said step of electroless deposition includes first immersing said substrate in a solution of metal ions whereby a layer of nanoparticles of metal are formed on the surface of said conductor. Lee discloses in figures 1 – 8 second immersing said substrate in an electroless complexed solution of metal ions and dimethylamino borane whereby the conductive film formed comprises a layer of metal-boron conductive film on said upper surface of said conductor. Lee teaches that the metal boron conductive film is a barrier layer. It is not clear if Lee and Hong teach annealing the metal boron conductive film. Zhao teaches in figure 13; column 3, lines 30 – 35; and column 8, lines 63 – 65 annealing a substrate in an inert atmosphere at a temperature of 200° C for 1 hour whereby excellent adhesion is obtained between a conductor (23) and a metal conductive film (24). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the annealing of Zhao in the method of Lee in order to improve the electrical properties of the plugs as stated by Zhao in column 3, lines 30 – 35. Lee, Hong, and Zhao discloses the claimed invention except for the anneal at a temperature of at least 300° C and a time of at least 2 hours. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the anneal at a temperature of at least 300° C and a time of at least 2 hours, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. It is further obvious in the method of Lee, Hong, and Zhao that excellent adhesion is obtained between the conductor and the metal-boron conductive film during the anneal.

With regard to claims 35 and 36, Lee teaches in column 7, line 59 wherein said conductive film is NiB.

Response to Arguments

11. Applicant's arguments filed January 22, 2003 have been fully considered but they are not persuasive.

12. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

13. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

14. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching,

suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, motivation for all of the proposed combinations have been provided in the rejections. Specifically particular sections of Hong (column 1, lines 32 – 36) and Zhao (column 3, lines 30 – 35) have been provided as motivation for the proposed combinations.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
February 27, 2003

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